MOCVD OF TiO_2 THIN FILM FOR USE AS FeRAM H_2 PASSIVATION LAYER

Inventors: Tingkai Li
Wei Pan
Robert Barrowcliff
David Russell Evans
Sheng Teng Hsu

Field of the Invention

This invention relates to oxide thin film processes for H_2 passivation layers, ferroelectric memory device structures and integrated processes for ferroelectric non-volatile memory devices, and specifically, to a method of depositing a TiO_2 thin film which is used as an H_2 passivation layer.

Background of the Invention

Metal, Ferroelectrics, Insulator, and Silicon (MFMIS) and Metal, Ferroelectrics, Insulator, and Silicon (MFIS) transistor ferroelectric memory devices have been proposed for use as FeRAM devices. In the integration processes of such devices, forming gas annealing generally is necessary to reduce trapped charges in high-k gate oxides and to improve the contact between metal connections and the source and the drain. However, forming gas annealing degrades the properties of ferroelectric thin films. Therefore, a H_2 passivation layer, covering the ferroelectric thin film, is an important structure in fabrication of 1T ferroelectric memory devices.

Summary of the Invention

A method of forming an H_2 passivation layer in an FeRAM includes preparing a silicon substrate; depositing a layer of TiO_x thin film, where $0<x<2$, on a damascene structure; plasma space etching of the TiO_x thin film to form a TiO_x sidewall; annealing the TiO_x side wall

thin film to form a TiO_2 thin film; depositing a layer of ferroelectric material; and metallizing the structure to form a FeRAM.

It is an object of the invention to provide a TiO_2 thin film as a H_2 passivation layer for improving the properties of 1 T ferroelectric memory devices.

Another object of the invention is to provide a TiO_x thin film having good step coverage on a damascene structure.

A further object of the invention is to use a plasma space etching process on a TiO_x thin film to form a TiO_2 thin film as a H_2 passivation layer.

This summary and objectives of the invention are provided to enable quick comprehension of the nature of the invention. A more thorough understanding of the invention may be obtained by reference to the following detailed description of the preferred embodiment of the invention in connection with the drawings.

Brief Description of the Drawings

Figs. 1-8 depict steps in device formation according to the method of the invention.

Figs. 9 and 10 are microphotographs of the structure during device fabrication.

Detailed Description of the Preferred Embodiments

In the method of the invention, TiO_x may be deposited in either of two embodiments to make TiO_2 as a H_2 passivation layer. In the first embodiment of the method of the invention, a CVD process is used to deposit Ti or TiO_x thin films on a damascene structure, providing good step coverage, followed by plasma space etching of the TiO_x thin film to form a TiO_x sidewall, and annealing the TiO_x side wall thin film to form a TiO_2 thin film. The second embodiment of the method of the invention includes a CVD process to deposit a TiO_x or TiO_2 thin

film on a damascene structure, again providing good step coverage, annealing the TiO_x thin film to form a TiO_2 thin film, and plasma space etching the TiO_2 thin film to form a sidewall on the trench structure.

Referring initially to Fig. 1, a silicon wafer 10 is prepared for fabrication of IC devices, which preparation may include doping to form a P-type silicon wafer, including threshold adjustment ion implantation, for use as a substrate for a Lead Germanium Oxide ($Pb_5Ge_3O_{11}$) (PGO) MFMPOS one-transistor FeRAM device. Fig. 1 depicts the structure following wafer preparation, STI and filling of the trenches so formed with oxide 12, growth of a gate oxide 14 and deposition of a polysilicon layer 16, and, in this example, ion implantation to form an N^+ source 18 and an N^+ drain 20. The oxide is smoothed by CMP, photoresist is applied and the polysilicon layer etched.

Fig. 2 depicts the structure following CVD of oxide, which is smoothed by CMP, stopping at the level of polysilicon layer 16. A larger size bottom electrode 22, which, in the preferred embodiment, is an Iridium electrode is deposited and patterned. Another layer of oxide 24 is deposited by CVD and smoothed by CMP, stopping at the level of the Iridium layer. tetraethylorthosilicate oxide (oxane or TEOS) 26 is deposited by CVD, patterned and etched to form trench structures.

Fig. 3 depicts the structure following CVD of a TiO_x layer 28, where $0<x<2$. As will be apparent to those of skill in the art, when $x=0$, the CVD is only of titanium. The MOCVD process includes preparing a MOCVD precursor, including dissolving 0.2 mol $Ti(OC_3H_7)_4$ in Octane, resulting in a precursor solution having a concentration of 0.2 mol $Ti(OC_3H_7)_4$. The precursor solution is injected into a vaporizer at temperature in the range of between about 80°C to

120°C by a liquid controller at a rate of between about 0.1 ml/min to 0.5 ml/min to form a precursor gases. The feed line is maintained at between about 80°C to 120°C, the deposition temperature is between about 380°C to 420°C, the deposition pressure is maintained at between about 0.5 torr to 5 torr, and the deposition time ranges from between about five minutes to thirty minutes, depending on the required TiO_2 thickness. TiO_x layer 28 may be, in the first embodiment of the method of the invention, plasma space etched, then annealed in an oxygen atmosphere to form a TiO_2 thin film. The structure is HF dipped to clean the surface of Iridium bottom electrode 20, resulting in the structure depicted in Fig. 4. The plasma space etching process for TiO_x thin film 22 includes setting TCP Rf power at about 370W and setting the bias power to about 130 W at a chamber pressure of about 5 torr. The etching chemicals used in the process include BCl_3 at a flow rate of about 30 sccm, and Cl_2 at a flow rate of about 58 sccm.

Fig. 5 depicts the structure following selective deposition of a ferroelectric thin film 24 by MOCVD. The upper surface of the FE and TiO_x extend above the level of the lastly deposited oxide layer because PGO may be selectively deposited on iridium and TiO_2, but will not form on SiO_2, therefor, the PGO will only be deposited on those areas which have exposed iridium and TiO_2.

Fig. 6 depicts the structure following CMP of ferroelectric thin film 30, surrounding TiO_x 28, and oxide 26.

Fig. 7 depicts the structure following deposition and annealing of a high-k oxide 32, deposition of a top electrode layer 34, and patterning and etching of the top electrode layer to form top electrodes 34.

Fig. 8 depicts the FeRAM constructed according to the first embodiment of the

method of the invention following etching of contact holes and metallization 36.

Fig. 9 depicts the structure following deposition of TiO_x thin film layer 28, which illustrates deposition on oxide trench structures with very good step coverage.

Fig. 10 depicts the structure after plasma space etching, and illustrates the TiO_x side wall thin film formed on oxide trench structures.

In the second embodiment of the method of the invention, the same processes are followed, as described in connection with Figs. 1-3. The annealing step, described in connection with Fig. 7, is next performed, converting TiO_x to TiO_2, which is then followed by the steps described in connection with Figs. 4-6 and 8.

Thus, a method for MOCVD TiO_2 thin film as FeRAM H_2 passivation layer has been disclosed. It will be appreciated that further variations and modifications thereof may be made within the scope of the invention as defined in the appended claims.